vADC5_S_T work in progress

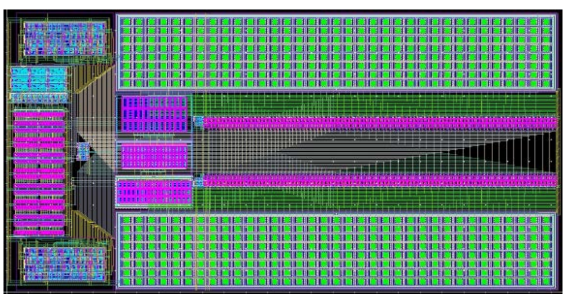
Differential SAR-Based Voltage-Mode Synchronous ADC with S/H

Proof of silicon due 1Q25 | Simulation results below

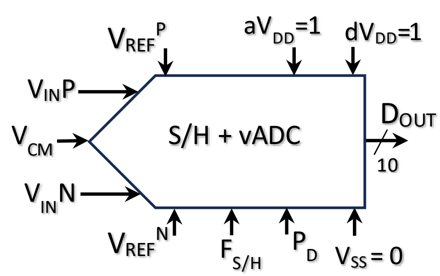
Parameter (units)	Typical Simulation Spec	**Typical Conditions:** V_{DD}=1v, Temperature = 27C, unless otherwise stated. Operating V_{DD} high ≈1v, Operating V_{DD} low ≈TBD,
Resolution (Bits)	8	
Differential V_{IN} peak-to-peak (v)	0⟶V_{REF}	V_{REF}P ≈1v & V_{REF}N ≈0v, V_{CM} ≈ 0.5xV_{DD}
I_{DD} (µA)	~1.1	$f_{S/H}$ ≈ 40KHz
ENOB (bits)	~7.5	V_{IN} sweep 0→Full-Scale
Gain Error (%)	~30	V_{IN} sweep 0→Full-Scale
Input Bandwidth = AIN_{BW} (KHz)	25	-3dB frequency
$f_{S/H}$ max (KHz)	tbd	1-bit Loss of ENOB
Digital I/O Levels (v)	0⟶V_{DD}	
Cell Size (µm X µm)	~127x64	
TSMC Process Node (nm)	65	

See Disclaimers

vADC +S/H Cell Layout



vADC +S/H Block Diagram



Features:

- 8-bit resolution, Low-Power, Differential voltage-input, Synchronous vADC with S/H & Power-Down
- Optional: Digital output port (D_{OUT}) can be serialized as needed.
- Digital power consumption reduces dynamically in steady-state V_{IN} conditions, enabled by asynchronous vADC architecture.
- V_{IN}P and V_{IN}N terminals swing ~1v Peak-to-Peak around common mode voltage (e.g., V_{CM} ≈ 0.5xV_{DD})
- Operating condition example: V_{REF}P ≈ 1v and V_{REF}N ≈ 0v