

# vADC5\_A\_T work in progress

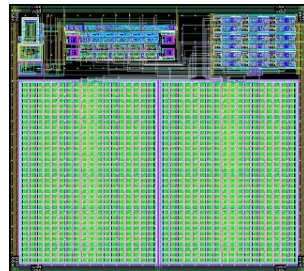
## Differential SAR-Based Voltage-Mode Asynchronous ADC with S/H

Proof of silicon due 1Q25 | Simulation results below

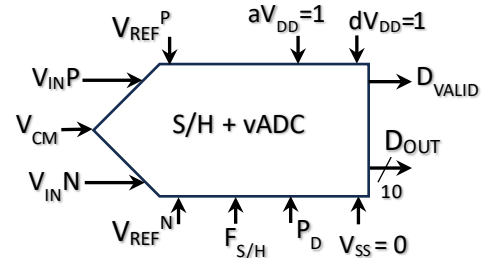
Parameter (units)	Typical Simulation Spec	Typical Conditions: $V_{DD}=1v$ , Temperature = 27C, unless otherwise stated. Operating $V_{DD}$ high $\approx 1v$ , Operating $V_{DD}$ low $\approx TBD$ ,
Resolution (Bits)	10	
Differential $V_{IN}$ peak-to-peak (v)	$0 \rightarrow V_{REF}$	$V_{REFP} \approx 1v$ & $V_{REFN} \approx 0v$ , $V_{CM} \approx 0.5xV_{DD}$
$I_{DD}$ ( $\mu A$ )	$\sim 1.5$	$f_{S/H} \approx 40KHz$
ENOB (bits)	$\sim 9.7$	$V_{IN}$ sweep $0 \rightarrow Full-Scale$
Gain Error (%)	$\sim 30$	$V_{IN}$ sweep $0 \rightarrow Full-Scale$
Input Bandwidth = $A_{INBW}$ (KHz)	15	-3dB frequency
$f_{S/H}$ max (KHz)	tbd	1-bit Loss of ENOB
Digital I/O Levels (v)	$0 \rightarrow V_{DD}$	
Cell Size ( $\mu m \times \mu m$ )	$\sim 112x101$	
TSMC Process Node (nm)	65	

\*See Disclaimers\*

vADC +S/H Cell Layout



vADC +S/H Block Diagram



### Features:

- 10-bit resolution, Low-Power, Differential voltage-input, Asynchronous vADC with S/H & Power-Down
- Optional: Digital output port ( $D_{OUT}$ ) can be serialized as needed.
- Digital power consumption reduces dynamically in steady-state  $V_{IN}$  conditions, enabled by asynchronous vADC architecture.
- $V_{INP}$  and  $V_{INN}$  terminals swing  $\sim 1v$  Peak-to-Peak around common mode voltage (e.g.,  $V_{CM} \approx 0.5xV_{DD}$ )
- Example:  $V_{REFP} \approx 1v$  and  $V_{REFN} \approx 0v$