iADC4_4

iADC: Patented Ultra-Low-Power Pseudo-FLASH Current I_{IN} Asynchronous iADC: P-Type

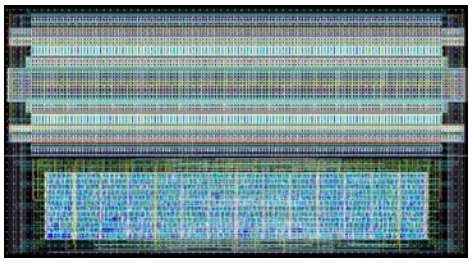
Proof of silicon: 4Q24 | IC testing in progress | Simulation results below

Please contact sales@ailinear.com for more information & ordering specific evaluation.

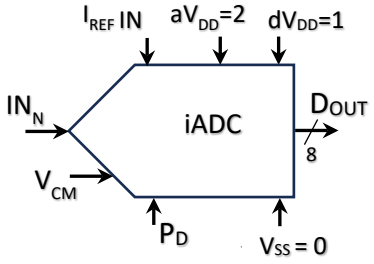
Parameter (units)	**Typical Simulation Spec**	**Typical Conditions:** V_{DD}=2v, Temperature = 27C, unless otherwise stated
Resolution (Bits)	8	
I_{IN} peak-to-peak (nA)	0→I_{REF}	I_{REF}≈256nA. I_{IN} Compliance voltage V_{CM}: V_{GS} from rail
aV_{DD} High (v)	~2	
aV_{DD} Low (v)	~1	aV_{DD} sweep 0v→2v
I_{DD} (nA)	~850	I_{IN} ≈ full-scale. I_{REF}≈256nA
Integral non-linearity = INL (LSB)	~±0.7	I_{IN} sweep 0→Full-Scale
Gain Error (LSB)	~±4	I_{IN} sweep 0→Full-Scale
Input Bandwidth = AIN_{BW} (KHz)	tbd	-3dB frequency
Transient Time = T (µS)	4	D_{OUT} time from I_{IN} 1µS pulse ¼ to ¾ scale
Digital I/O Levels (v)	0→dV_{DD}	
Cell Size (µm X µm)	~335x180	
TSMC Process Node (nm)	180	

See Disclaimers

iADC Cell Layout



iADC Block Diagram



Features:

- Patent P-Type iADC with Pseudo-FLASH architecture enhances accuracy and speed, reducing power consumption (I_{DD}), footprint, and cost.
- The iADC is Inherently Monotonic, with Bubble Error Correction
- Optional: Digital output port (D_{OUT}) can be serialized as needed.
- Digital power consumption reduces dynamically in steady-state I_{IN} conditions, enabled by asynchronous iADC architecture.
- iADC includes power-down (P_D) capabilities.