

iADC4_3

iADC: Patented Ultra-Low-Power Pseudo-FLASH Current I_{IN} Asynchronous iADC: N-Type

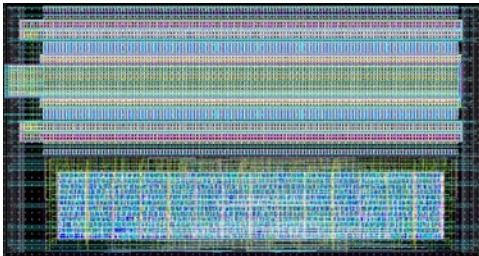
Proof of silicon: 4Q24 | IC testing in progress | Simulation results below

Please contact sales@ailinear.com for more information & ordering specific evaluation.

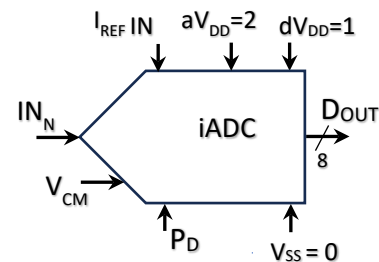
Parameter (units)	Typical Simulation Spec	Typical Conditions: $V_{DD}=2v$, Temperature = 27C, unless otherwise stated
Resolution (Bits)	8	
I_{IN} peak-to-peak (nA)	$0 \rightarrow I_{REF}$	$I_{REF} \approx 256nA$. I_{IN} Compliance voltage V_{CM} : V_{GS} from rail
a V_{DD} High (v)	~ 2	
a V_{DD} Low (v)	~ 1	a V_{DD} sweep $0v \rightarrow 2v$
I_{DD} (nA)	~ 2100	$I_{IN} \approx$ full-scale. $I_{REF} \approx 256nA$
Integral non-linearity = INL (LSB)	$\sim \pm 0.5$	I_{IN} sweep $0 \rightarrow$ Full-Scale
Gain Error (LSB)	$\sim \pm 6$	I_{IN} sweep $0 \rightarrow$ Full-Scale
Input Bandwidth = $A_{IN_{BW}}$ (KHz)	tbd	-3dB frequency
Transient Time = τ (μs)	4	D_{OUT} time from I_{IN} $1\mu s$ pulse $\frac{1}{4}$ to $\frac{3}{4}$ scale
Digital I/O Levels (v)	$0 \rightarrow dV_{DD}$	
Cell Size ($\mu m \times \mu m$)	$\sim 345 \times 180$	
TSMC Process Node (nm)	180	

See Disclaimers

iADC Cell Layout



iADC Block Diagram



Features:

- Patent N-Type iADC with Pseudo-FLASH architecture enhances accuracy and speed, reducing power consumption (I_{DD}), footprint, and cost.
- The iADC is Inherently Monotonic, with Bubble Error Correction
- Optional: Digital output port (D_{OUT}) can be serialized as needed.
- Digital power consumption reduces dynamically in steady-state I_{IN} conditions, enabled by asynchronous iADC architecture.
- iADC includes power-down (P_D) capabilities.