iADC3_4

iADC: Experimental Sub-Ranging Current-Mode Current I_{IN} Asynchronous Ultra-Low-Power iADC

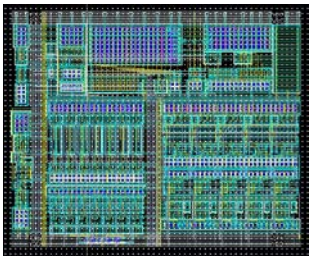
Proof of silicon: 4Q24 | IC testing in progress | Simulation results below

Please contact sales@ailinear.com for more information & ordering specific evaluation.

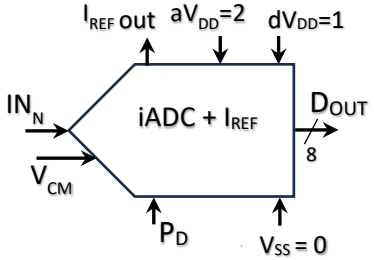
Parameter (units)	Typical Simulation Spec	Typical Conditions: V_{DD}=2v, Temperature = 27C, unless otherwise stated
Resolution (Bits)	8	
I_{IN} peak-to-peak (nA)	0⟶I_{REF}	I_{REF} ≈256nA
V_{CM} (v)	0.5xaV_{DD}	I_{IN} current source compliance voltage (rails ±V_{GS})
I_{REF} Output (nA)	25.6	
aV_{DD} High (v)	~2	
aV_{DD} Low (v)	~1	aV_{DD} sweep 0v→2v
I_{DD} (nA)	~885	I_{IN} ≈ full-scale. I_{REF} ≈256nA
Integral Non-Linearity = INL (LSB)	~±1.5	I_{IN} sweep 0→Full-Scale
Gain Error (LSB)	~±10	I_{IN} sweep 0→Full-Scale
Input Bandwidth = AIN_{BW} (KHz)	tbd	-3dB frequency
Transient Time = τ (µS)	38	D_{OUT} time from I_{IN} pulse ¼ to ¾ scale in 1µS
Digital I/O Levels (v)	0⟶dV_{DD}	
Cell Size (µm X µm)	~290x240	
TSMC Process Node (nm)	180	

See Disclaimers

iADC + I_{REF} Cell Layout



iADC + I_{REF} Block Diagram



Features:

- Patented segmented sub-ranging iADC. Thermometer-based Most-Significant-Portion (MSP) of iADC's first stage reference network inherently enhances the accuracy of the overall iADC
- Optional: Programmable internal I_{REF} customizes I_{IN} peak-to-peak ranges, supporting range calibration via I_{REF} output.
- Optional: Digital output port (D_{OUT}) can be serialized as needed.
- Digital power consumption reduces dynamically in steady-state I_{IN} conditions, enabled by asynchronous iADC architecture.
- iADC includes power-down (P_D) and I_{IN} current source compliance (V_{CM}) voltage setting capabilities.