$V_{REF}8$ (internal #chip2_DTMOST)

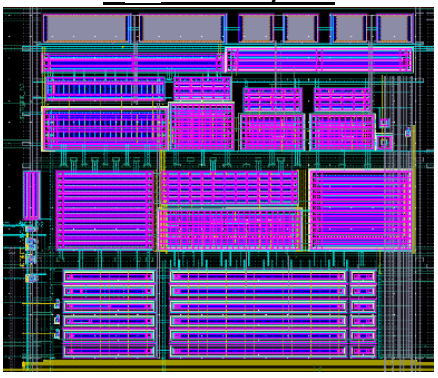
Ultra-Low-Power Fractional Voltage Reference with low TC. Proof of silicon with typical/preliminary measurements available.

Please contact sales@ailinear.com for more information & order specific evaluation

Parameter	Typical Spec	Condition
I_{DD} (nA)	~49	V_{DD}=1v, Temperature = 27C
V_{DD} Low (v)	~0.7	V_{DD}=1v, Temperature = 27C
V_{DD} High (v)	~1	V_{DD} sweep 0v→1.1v, Temperature = 27C
$VREF_{OUT}$ (v)	~0.43	V_{DD}=1v, Temperature = 27C
TC (PPM/C)	TBD	Test in progress. See Disclaimer
PSRR (dB)	TBD	Test in progress. See Disclaimer

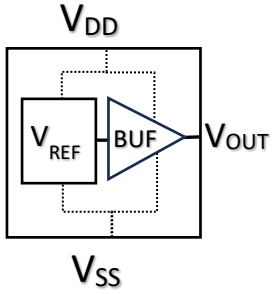
See Disclaimer

V_{REF} Cell Layout



V_{REF} Cell Size ~100µm×82 µm in TSMC 65nm CMOS

V_{REF} Block Diagram



Features:

- Small CMOS (~100µm×82 µm) bandgap voltage reference ($V_{OUT} \approx V_{REF} \approx 0.43$) Intellectual Property (IP) cell operates in subthreshold with ultra-low I_{DD} (typical 49nA)
- Patented Low noise design to generate proportional to absolute voltage (V_{PTAT}) without resistors
- Equipped with start-up, power-down, and TC trim capability
- Includes an internal buffer (BUF) to drive larger loads (e.g. Mega Ωs) in a SoC
- No clock, no switch-capacitor, and no related noise or injections into substrate
- Operating in subthreshold and requiring no resistors facilitate small silicon area and operations at ultra-low currents
- Operation at low V_{DD} levels ≈V_{REF} + 2V_{DS}
- Manufacturable on trailing-to-bleeding edge digital CMOS
- Based on 65nm digital CMOS at TSMC and portable to smaller fabrication nodes.