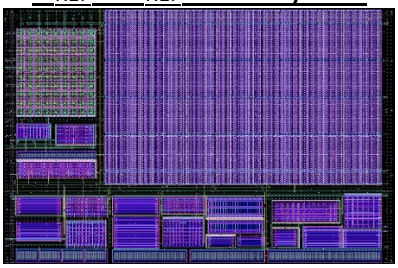
$V_{REF}7$ (internal #chip2_VBGF)

Fractional Bandgap Voltage & Current Reference with low TC. Proof of silicon with typical/preliminary measurements available. Please contact sales@ailinear.com for details & order specific evaluation

Parameter	Typical Spec	Condition
I_{DD} (nA)	~330	V_{DD}=1v, Temperature = 27C
V_{DD} Low (v)	~0.8	V_{DD} sweep 0v→1.1v, Temperature = 27C
V_{DD} High (v)	~1	V_{DD} sweep 0v→1.1v, Temperature = 27C
$VREF_{OUT}$ (v)	~0.63	V_{DD}=1v, Temperature = 27C
$IREF_{OUT}$ (v)	~50	V_{DD}=1v, Temperature = 27C
VREF TC (PPM/C)	TBD	Test in progress
IREF TC (PPM/C)	TBD	Test in progress
VREF PSRR (dB)	TBD	Test in progress

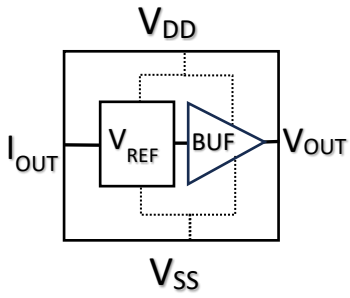
See Disclaimer

V_{REF} & I_{REF} Cell Layoutf



V_{REF} & I_{REF} Cell Size ~200µm×130 µm in TSMC 65nm CMOS

V_{REF} & I_{REF} Block Diagram



Features:

- CMOS (~200µm×130 µm) fractional bandgap voltage and current reference ($V_{REF} \approx V_{OUT} \approx 0.5V_{BG} \approx 0.63$ & typ. $I_{REF} \approx I_{OUT} \approx 50$nA) Intellectual Property (IP) cell operates in subthreshold with low I_{DD} (typical 330nA)
- Trimmable or Programmable (pre or post silicon) absolute value of V_{REF} & I_{REF}
- Trimmable or Programmable TC
- Equipped with start-up, and power-down
- V_{REF} Includes an internal buffer (BUF) to drive larger loads (e.g. Mega Ωs) in a SoC
- No clock, no switch-capacitor, and no related noise or injections into substrate
- Utilizes a fractional bandgap topology to generate V_{REF} & I_{REF} through a bias resistor (R_{POLY})
- Operation at low V_{DD} levels ≈V_{REF} + 2V_{DS}
- Suitable for SoC optimized for V_{REF} & I_{REF} fractional bandgap voltage loop that is coupled to V_{SS}
- Utilizes parasitic (substrate) bipolar junction transistor (BJT) freely available in digital CMOS
- Based on 65nm digital CMOS at TSMC and portable to smaller fabrication nodes.