$V_{REF}5$ (internal #chip3_VBGF1)

Fractional Bandgap Voltage Reference with low TC.

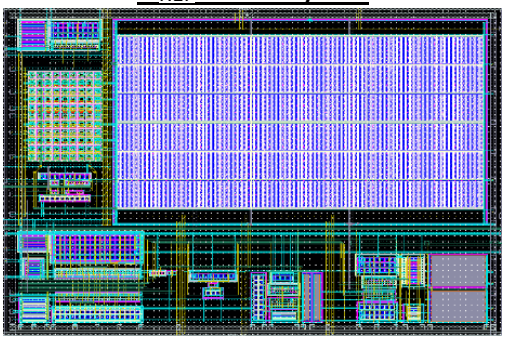
Proof of silicon with typical/preliminary measurements available.

Please contact sales@ailinear.com for more information & order specific evaluation

Parameter	Typical Spec	Condition
I_{DD} (nA)	~270	V_{DD}=2v, Temperature = 27C
V_{DD} Low (v)	~1	V_{DD} sweep 0v→2.2v, Temperature = 27C
V_{DD} High (v)	~2	V_{DD} sweep 0v→2.2v, Temperature = 27C
$VREF_{OUT}$ (v)	~0.63	V_{DD}=2v, Temperature = 27C
TC (PPM/C)	TBD	Test in progress
PSRR (dB)	TBD	Test in progress

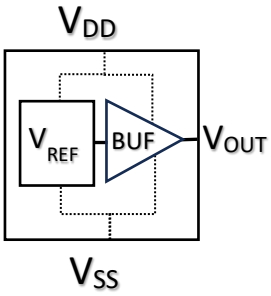
See Disclaimer

V_{REF} Cell Layout



V_{REF} Cell Size ~460µm×250 µm in TSMC 180nm CMOS

V_{REF} Block Diagram



Features:

- CMOS (~460µm×250 µm) fractional bandgap voltage reference ($V_{OUT} \approx V_{REF} \approx 0.5V_{BG} \approx 0.63$) Intellectual Property (IP) cell operates in subthreshold with low I_{DD} (typical 270nA)
- Trimmable or Programmable (pre or post silicon) absolute value of V_{REF}
- Trimmable or Programmable TC
- Equipped with start-up, and power-down
- Includes an internal buffer (BUF) to drive larger loads (e.g. Mega Ωs) in a SoC
- No clock, no switch-capacitor, and no related noise or injections into substrate
- Utilizes a fractional bandgap topology to generate I_{REF} through a bias resistor (R_{POLY})
- Operation at low V_{DD} levels ≈V_{REF} + 2V_{DS}
- Suitable for SoC optimized for I_{REF} fractional bandgap voltage loop that is coupled to V_{SS}
- Utilizes parasitic (substrate) bipolar junction transistor (BJT) freely available in digital CMOS
- Based on 180nm digital CMOS at TSMC and portable to smaller fabrication nodes.