

# VREF4

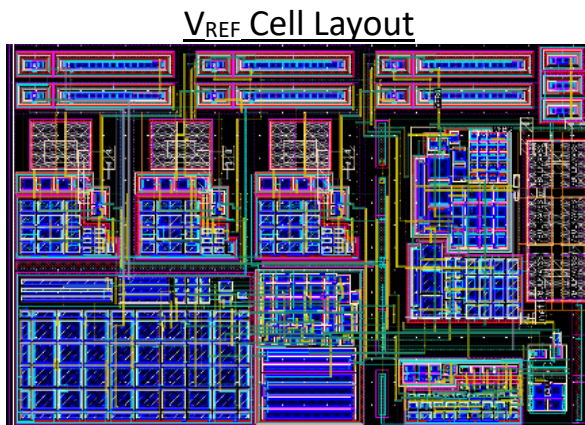
(internal #chip1\_DT MOST4)

Ultra-Low-Power Fractional Voltage Reference with low TC. Proof of silicon with typical/preliminary measurements available.

Please contact [sales@ailinear.com](mailto:sales@ailinear.com) for more information & order specific evaluation

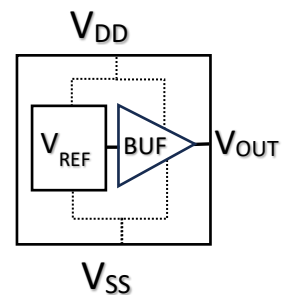
Parameter	Typical Spec	Condition
$I_{DD}$ (nA)	~29	$V_{DD}=2V$ , Temperature = 27C
$V_{DD}$ Low (v)	~0.7	$V_{DD}$ sweep 0v→2.2v, Temperature = 27C
$V_{DD}$ High (v)	~2	$V_{DD}$ sweep 0v→2.2v, Temperature = 27C
$V_{REF_{OUT}}$ (v)	~0.43	$V_{DD}=2V$ , Temperature = 27C
TC (PPM/C)	~230	$V_{DD}=2V$ , $\Delta T \sim 30C$
PSRR (dB)	~69	$V_{DD}$ sweep 1v→2.2v, Temperature = 27C

\*See Disclaimer\*



V<sub>REF</sub> Cell Size ~132μm×87 μm in TSMC 180nm CMOS

V<sub>REF</sub> Block Diagram



## Features:

- Small CMOS (~132μm×87 μm) bandgap voltage reference ( $V_{OUT} \approx V_{REF} \approx 0.43V$ ) Intellectual Property (IP) cell operates in subthreshold with ultra-low  $I_{DD}$  (typical 29nA)
- Patented Low noise design to generate proportional to absolute voltage ( $V_{PTAT}$ ) without resistors
- Equipped with start-up, power-down, and TC trim capability
- Includes an internal buffer (BUF) to drive larger loads (e.g. Mega Ωs) in a SoC
- No clock, no switch-capacitor, and no related noise or injections into substrate
- Operating in subthreshold and requiring no resistors facilitate small silicon area and operations at ultra-low currents
- Operation at low  $V_{DD}$  levels  $\approx V_{REF} + 2V_{DS}$
- Manufacturable on trailing-to-bleeding edge digital CMOS
- Based on 180nm digital CMOS at TSMC and portable to smaller fabrication nodes.