$I_{REF}8$ (internal #chip3_IREF_BG)

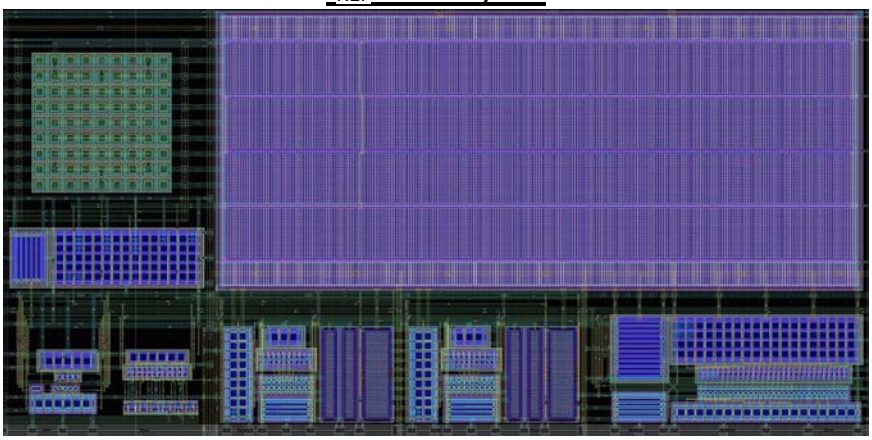
Low-Power Fractional Bandgap Current Reference with low TC. Proof of silicon with typical/preliminary measurements available.

Please contact sales@ailinear.com for more information & order specific evaluation

Parameter	Typical Spec	Condition
IDD (nA)	~160	V_{DD}=2v, Temperature = 27C
IREF (nA)	~55	V_{DD}=2v, Temperature = 27C
V_{DD} Low (v)	~1	V_{DD} sweep 0v→2.2v, Temperature = 27C
V_{DD} High (v)	~2	V_{DD} sweep 0v→2.2v, Temperature = 27C
TC (%/C)	TBD	V_{DD}=2v, ΔT ~30C. Test in progress
VC (%/V)	TBD	V_{DD} sweep 1v→2.2v, Temperature = 27C. Test in progress

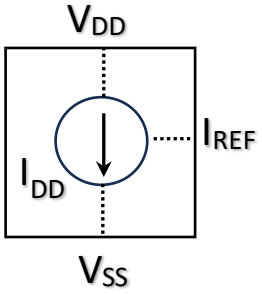
See Disclaimer

I_{REF} Cell Layout



I_{REF} Cell Size ~420µm×220 µm in TSMC 180nm CMOS

I_{REF} Block Diagram



Features:

- Trimmable or Programmable (pre or post silicon) absolute value of I_{REF}
- Trimmable or Programmable TC
- Equipped with start-up, power-down, and TC trim capability
- CMOS (~420µm×220 µm) bias current Intellectual Property (IP) cell operating in subthreshold with ultra-low current consumption I_{DD} (typical 55nA)
- Utilizes a fractional bandgap topology to generate I_{REF} through a bias resistor (R_{POLY})
- Suitable for SoC optimized for I_{REF} fractional bandgap voltage loop that is coupled to V_{SS}
- I_{DD} and I_{REF} absolute value mostly a function of R_{POLY}
- Based on 180nm digital CMOS at TSMC and portable to smaller fabrication nodes.