

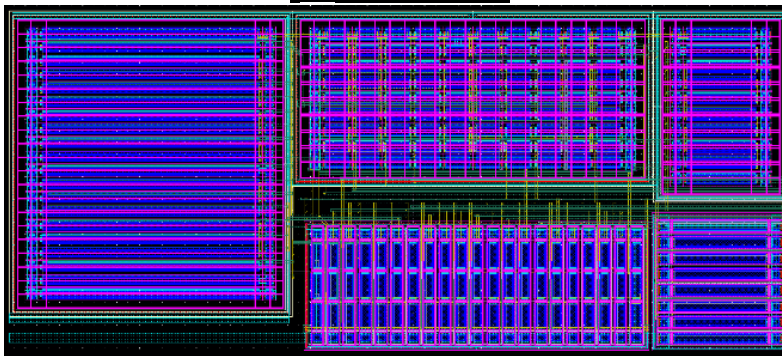
IREF2 (internal chip2_IREF2)

Ultra-Low-Power Reference Current with low TC. Proof of silicon with typical/preliminary measurements available. (Please contact sales@ailinear.com for more information)

Parameter	Typical Spec	Condition
I_{DD} (nA)	~74	$V_{DD}=1v$, Temperature = 27C
V_{DD} Low (v)	~0.7	V_{DD} sweep $0v \rightarrow 1.1v$, Temperature = 27C
V_{DD} High (v)	~1	V_{DD} sweep $0v \rightarrow 1.1v$, Temperature = 27C
TC (%/C)	~TBD	$V_{DD}=1v$, $\Delta T \sim 30C$
VC (%/V)	~TBD	V_{DD} sweep $1v \rightarrow 1.1v$, Temperature = 27C

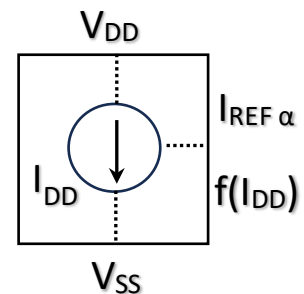
See Disclaimer

IREF Cell Layout



IREF Cell Size $\sim 70\mu m \times 30\mu m$ in TSMC 65nm CMOS

IREF Block Diagram



Features:

- Programmable (pre or post silicon) I_{REF} that tracks I_{DD}
- Tiny CMOS ($\sim 70\mu m \times 30\mu m$) bias current Intellectual Property (IP) cell operating in subthreshold with ultra-low current consumption I_{DD} (typical 74nA)
- Large value but tiny active bias resistor (R_{PMOS}) as a function of PMOSFET keeps I_{DD} ultra-low
- Most suitable for SoC whose analog (e.g., oscillator, comparator, ADC) performance best correlates with PMOSFET parameters
- Utilizing cascode current mirrors ($1V_{GS}+2V_{DS}$) for lower operating V_{DD}
- Suitable for SoC optimized for I_{REF} voltage loop that is coupled to V_{DD}
- I_{DD} and I_{REF} absolute value mostly a function of PMOSFET mobility (μ) inherently more stable to help narrow I_{DD} variation over normal fabrication process corners
- Based on 65nm digital CMOS at TSMC and portable to smaller fabrication nodes.