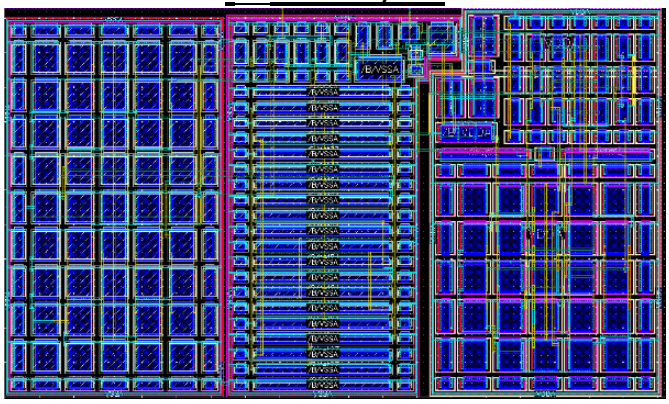
$I_{REF}1$ (internal chip2_IREF1)

Ultra-Low-Power Reference Current with low TC. Proof of silicon with typical/preliminary measurements available. (Please contact sales@ailinear.com for more information)

Parameter	Typical Spec	Condition
I_{DD} (nA)	~50	V_{DD}=1v, Temperature = 27C
V_{DD} Low (v)	~0.7	V_{DD} sweep 0v→1.1v, Temperature = 27C
V_{DD} High (v)	~1	V_{DD} sweep 0v→1.1v, Temperature = 27C
TC (%/C)	TBD	V_{DD}=1v, ΔT ~30C
VC (%/V)	TBD	V_{DD} sweep 1v→1.1v, Temperature = 27C

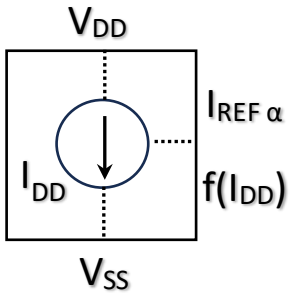
See Disclaimer

I_{REF} Cell Layout



I_{REF} Cell Size ~80µm×50 µm in TSMC 65nm CMOS

I_{REF} Block Diagram



Features:

- Programmable (pre or post silicon) I_{REF} that tracks I_{DD}
- Tiny CMOS (~80µm×50 µm) bias current Intellectual Property (IP) cell operating in subthreshold with ultra-low current consumption I_{DD} (typical 50nA)
- Large value but tiny active bias resistor (R_{NMOS}) as a function of NMOSFET keeps I_{DD} ultra-low
- Most suitable for SoC whose analog (e.g., oscillator, comparator, ADC) performance best correlates with NMOSFET parameters
- Utilizing cascode current mirrors ($1V_{GS}+2V_{DS}$) for lower operating V_{DD}
- Suitable for SoC optimized for I_{REF} voltage loop that is coupled to V_{SS}
- I_{DD} and I_{REF} absolute value mostly a function of NMOSFET mobility (µ) inherently more stable to help narrow I_{DD} variation over normal fabrication process corners
- Based on 65nm digital CMOS at TSMC and portable to smaller fabrication nodes.