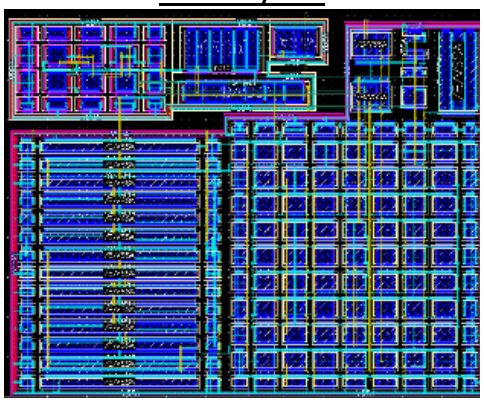
$I_{BIAS}5$

Ultra-Low-Power Proportional to Absolute Temperature (I_{PTAT}) Bias Current Source. Proof of silicon with typical/preliminary measurements available. (Please contact sales@ailinear.com)

Parameter	Typical Spec	Condition
I_{DD} (nA)	11	V_{DD}=2v, Temperature = 27C
V_{DD} Low (v)	0.8	V_{DD} sweep 0v→2.2v, Temperature = 27C
V_{DD} High (v)	2	V_{DD} sweep 0v→2.2v, Temperature = 27C
TC (%/C)	0.4	V_{DD}=2v, ΔT ~30C
VC (%/V)	0.5	V_{DD} sweep 1v→2.2v, Temperature = 27C

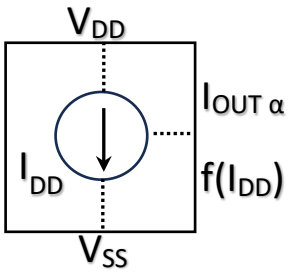
** see disclaimer

Cell Layout



Cell Size ~62µm×48 µm in TSMC 180nm CMOS

Block Diagram



Features:

- Patented
- Programmable (pre or post silicon) I_{OUT} that tracks I_{DD}
- Tiny CMOS (~62µm×48 µm) bias current Intellectual Property (IP) cell operating in subthreshold with ultra-low current consumption I_{DD} (typical 11nA)
- Large value but tiny active bias resistor (R_{NMOS}) as a function of NMOSFET keeps I_{DD} ultra-low
- Most suitable for SoC whose analog (e.g., oscillator, comparator, ADC) performance best correlates with NMOSFET parameters
- Suitable for SoC where I_{BIAS} is more optimized when V_{SS} coupled with PTAT Kirkoff Voltage Loop (KVL)
- Utilizing PTAT loop with NMOSFETs needing $1V_{GS}+2V_{DS}$ for lower V_{DD} operating range
- I_{DD} and I_{OUT} absolute value mostly a function of NMOSFET mobility (µ) inherently more stable to help narrow I_{DD} variation over fabrication process corners
- Based on 180nm digital CMOS at TSMC and portable to smaller fabrication nodes.