I$_{BIAS}$4

Ultra-Low-Power Proportional to Absolute Temperature (I$_{PTAT}$) Bias Current Source. Proof of silicon with typical/preliminary measurements available. (Please contact sales@ailinear.com)

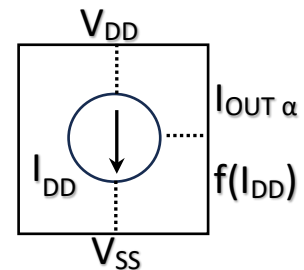| Parameter	Typical Spec	Condition
I$_{DD}$ (nA)	6	V$_{DD}$=2v, Temperature = 27C
V$_{DD}$ Low (v)	0.7	V$_{DD}$ sweep 0v→2.2v, Temperature = 27C
V$_{DD}$ High (v)	2	V$_{DD}$ sweep 0v→2.2v, Temperature = 27C
TC (%/C)	0.5	V$_{DD}$=2v, ΔT ~30C
VC (%/V)	0.5	V$_{DD}$ sweep 1v→2.2v, Temperature = 27C

** see disclaimer

Cell Layout
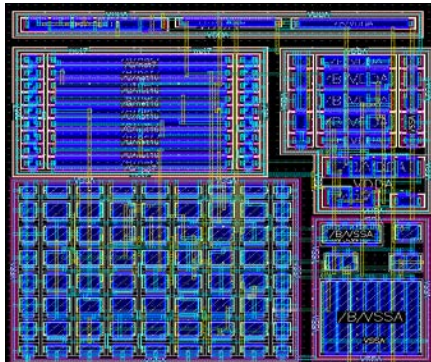
Cell Size ~48μm×50 μm in TSMC 180nm CMOS

Block Diagram

Features:

- Patented
- Programmable (pre or post silicon) I$_{OUT}$ that tracks I$_{DD}$
- Tiny CMOS (~48μm×50 μm) bias current Intellectual Property (IP) cell operating in subthreshold with ultra-low current consumption I$_{DD}$ (typical 6nA)
- Large value but tiny active bias resistor (R$_{PMOS}$) as a function of PMOSFET keeps I$_{DD}$ ultra-low
- Most suitable for SoC whose analog (e.g., oscillator, comparator, ADC) performance best correlates with PMOSFET parameters
- Suitable for SoC where I$_{BIAS}$ is more optimized when V$_{SS}$ coupled with PTAT Kirkoff Voltage Loop (KVL)
- Utilizing PTAT loop with NMOSFETs needing 1V$_{GS}$+2V$_{DS}$ for lower V$_{DD}$ operating range
- I$_{DD}$ and I$_{OUT}$ absolute value mostly a function of PMOSFET mobility (μ) inherently more stable to help narrow I$_{DD}$ variation over fabrication process corners
- Based on 180nm digital CMOS at TSMC and portable to smaller fabrication nodes.