Preliminary Data Sheet- IBIAS13_REV0

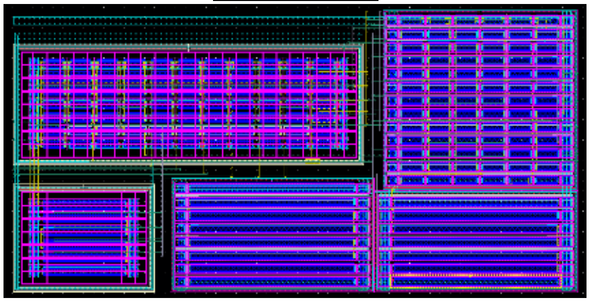
$I_{BIAS}13$

Ultra-Low-Power Proportional to Absolute Temperature (I_{PTAT}) Bias Current Source. Proof of silicon with typical/preliminary measurements available. (Please contact sales@ailinear.com)

Parameter	Typical Spec	Condition
I_{DD} (nA)	10	V_{DD}=1v, Temperature = 27C
V_{DD} Low (v)	0.6	V_{DD} sweep 0v→1.1v, Temperature = 27C
V_{DD} High (v)	1	V_{DD} sweep 0v→1.1v, Temperature = 27C
TC (%/C)	0.6	V_{DD}=1v, ΔT ~30C
VC (%/V)	0.5	V_{DD} sweep 0.6v→1.1v, Temperature = 27C

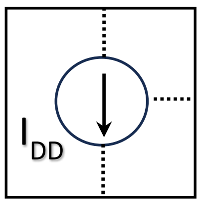
See Disclaimer

Cell Layout



Cell Size ~60µm×30 µm in TSMC 65nm CMOS

Block Diagram



Features:

- Programmable (pre or post silicon) I_{OUT} that tracks I_{DD}
- Tiny CMOS (~60µm×30 µm) bias current Intellectual Property (IP) cell operating in subthreshold with ultra-low current consumption I_{DD} (typical 10nA)
- Large value but tiny active bias resistor (R_{PMOS}) as a function of NMOSFET keeps I_{DD} ultra-low
- Most suitable for SoC whose analog (e.g., oscillator, comparator, ADC) performance best correlates with NMOSFET parameters
- Utilizing cascode current mirrors ($1V_{GS}+2V_{DS}$) for lower operating V_{DD}
- Suitable for SoC where I_{BIAS} is more optimized when PTAT Kirkoff Voltage Loop (KVL) is coupled to V_{SS}
- I_{DD} and I_{OUT} absolute value mostly a function of NMOSFET mobility (µ) inherently more stable to help narrow I_{DD} variation over fabrication process corners
- Based on 65nm digital CMOS at TSMC and portable to smaller fabrication nodes.