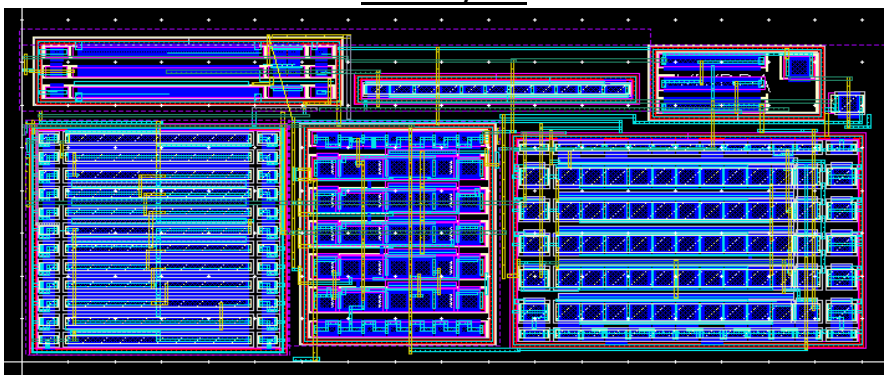
I_{BIAS}12L

Ultra-Low-Power Proportional to Absolute Temperature (I_{PTAT}) Bias Current Source. Proof of silicon with typical/preliminary measurements available. (Please contact sales@ailinear.com)

Parameter	Typical Spec	Conditions
I_{DD} (nA)	22	V_{DD}=2v, Temperature = 27C
V_{DD} Low (v)	0.8	V_{DD} sweep 0v→2.2v, Temperature = 27C
V_{DD} High (v)	2	V_{DD} sweep 0v→2.2v, Temperature = 27C
TC (%/C)	0.7	V_{DD}=2v, ΔT ~30C
VC (%/V)	0.4	V_{DD} sweep 1v→2.2v, Temperature = 27C

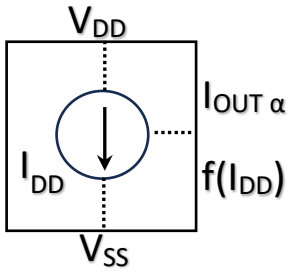
See Disclaimer

Cell Layout



Cell Size ~90µm×40 µm in TSMC 180nm CMOS

Block Diagram



Features:

- Programmable (pre or post silicon) I_{OUT} that tracks I_{DD}
- Tiny CMOS (~90µm×40 µm) bias current Intellectual Property (IP) cell operating in subthreshold with ultra-low current consumption IDD (typical 22nA)
- Large value but tiny active bias resistor (R_{PMOS}) as a function of PMOSFET keeps I_{DD} ultra-low
- Most suitable for SoC whose analog (e.g., oscillator, comparator, ADC) performance best correlates with PMOSFET parameters
- Utilizing peaking current mirrors ($1V_{GS}+2V_{DS}$) for lower voltage V_{DD} coefficient and lower operating V_{DD}
- Suitable for SoC where I_{BIAS} is more optimized when PTAT Kirkoff Voltage Loop (KVL) is coupled to V_{DD}
- I_{DD} and I_{OUT} absolute value mostly a function of PMOSFET mobility (µ) inherently more stable to help narrow I_{DD} variation over fabrication process corners
- Based on 180nm digital CMOS at TSMC and portable to smaller fabrication nodes.