AMP1_3

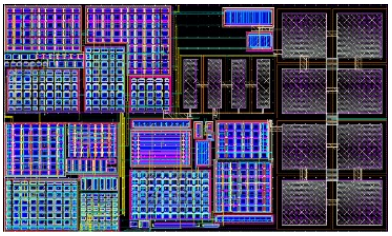
Smart Amplifier: Ultra-Low-Power, Low-Noise, High-Gain, Near Rail-To-Rail input/output (I/O), Moderate-Speed Buffer Amplifier. Proof of silicon with typical/preliminary measurements available.

Please contact sales@ailinear.com for more information & ordering specific evaluation.

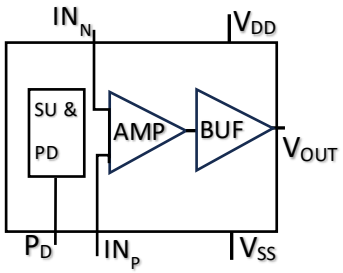
Parameter	Typical Spec	Typical Conditions: V_{DD}=2v, Temperature = 27C, unless otherwise stated
I_{DD} (nA)	~90	sAMP Gain=1 & $V_{INPUT} \approx 0.5\ V_{DD}$
V_{DD} Low (v)	~1.1	V_{DD} sweep 0v→2v
V_{DD} High (v)	~2	V_{DD} sweep 0v→2v
V_{OFFSET} (mv)	~±5	sAMP Gain=1 & $V_{INPUT} \approx 0.5\ V_{DD}$
I/O Swing to Rails (mv)	~±50	V_{DD} sweep 0v→2v
Gain (dB)	~85	sAMP Gain=1 & $V_{INPUT} \approx 0.5\ V_{DD}$. Tested at higher frequencies and extrapolated to DC
PSRR (dB)	~90	sAMP Gain=1 & $V_{INPUT} \approx 0.5\ V_{DD}$. Tested at higher frequencies and extrapolated to DC
Noise (µv/√Hz)	~4	V_{OUT} noise 10Hz. sAMP Gain=1 & $V_{INPUT} \approx 0.5\ V_{DD}$.
fu (KHz)	~1	sAMP Gain=1 & 10mv p-p V_{INPUT} mid $\approx 0.5\ V_{DD}$
SR (v/ms)	~72	sAMP Gain=1 & 1v p-p pulse V_{INPUT} mid $\approx 0.5\ V_{DD}$
ts (µs)	~50	sAMP Gain=1 & 1v p-p pulse V_{INPUT} mid $\approx 0.5\ V_{DD}$
Cell Size (µm X µm)	~105x190	
TSMC Process Node (nm)	180	

See Disclaimers

sAMP Cell Layout



sAMP Block Diagram



Features:

- The sAMP's $I_Q \approx f(PTAT) \rightarrow$ improved dynamic response's TC
- The $I_{DD} \approx f(I_Q) \approx f(\mu_{PMOS}) \approx f(R_{PMOS}) \neq f(V_{TH}) \rightarrow I_{DD}$ less sensitive to manufacturing variations
- The R_{PMOS} inside PTAT voltage loop coupled to V_{SS} for lower V_{DD} noise sensitivity
- At ultra-low I_{DD}, utilizing regulated cascode gain boosting in the FCTA stage
- The sAMP with internal class AB (push-pull) buffer (BUF) can drive larger loads (e.g. 10s of mega Ωs) in a low-power SoC