Santana Row, 3031 Tisch Way, 110 Plaza West, PMB#: 220, San Jose, CA 95128

POSITION:

Back-End Digital IC Design Engineer

RESPONSIBILITIES:

- Floorplan, place & route hybrid (analog & digital) chips
- LVS/DRC/ERC silicon signoff, LEC behavioral vs. gate, electrical signoff (IR drop, antenna, cap fill, etc.)
- Work closely with layout designers as needed
- Work closely with Product Test engineers to develop production test plan
- Work closely with Packaging Engineers to plan package design.
- Release GDS2 to Foundry

REQUIRED QUALIFICATIONS:

- BSEE/CS or MSEE/CS and 5+ years of hands-on back-end digital Design experience (having released digital ASICs/SoCs to production).
- Demonstrated ability to floorplan, place, & route digital chips.
- Experience with both LVS, DRC, ERC, and LEC tools
- Experience with Verilog gate-level modeling.
- Good organization; written and verbal communication skills

DESIRED QUALIFICATIONS:

- Good background with RTL-to-GDS flow (either Synopsys, Cadence, or Mentor)
- Ultra-low power digital design techniques, including clock and power gating
- Clock tree routing, scan chain routing
- SPEF generation