Santana Row, 3031 Tisch Way, 110 Plaza West, PMB#: 220, San Jose, CA 95128

POSITION:

Digital IC Design Verification Engineer

RESPONSIBILITIES:

- **Test plans, test bench construction & test vector construction**
- **Use Synopsys Verdi or Cadence vManager to keep track of functional coverage.**
- **Collaborate with Software, Systems, Analog, and Applications Engineers to meet customer needs.**
- **Collaborate with product engineers to design-for-test, including test insertion (e.g., scan, JTAG, MBIST) and test pattern generation.**

REQUIRED QUALIFICATIONS:

- **BSEE/CS or higher and 3+ years of hands-on digital CMOS IC/SoC Design experience**
- **Experience with System Verilog and UVM verification methodology**
- **Good organization; written and verbal communication skills**

DESIRED QUALIFICATIONS:

- **Strong scripting skills (Python or Perl)**
- **Experience with FPGA-based emulation and/or Cadence Palladium.**
- **Experience with Cadence Jasper (formal).**
- **Experience with bug tracking tools such as Atlassian Jira**