Santana Row, 3031 Tisch Way, 110 Plaza West, PMB#: 220, San Jose, CA 95128

POSITION:

Digital RTL IC Design Engineer

RESPONSIBILITIES:

- Develop ultra-low power hybrid (analog & digital) IoT interface chips, architecture through production
- Develop functional specifications, coordinate on functional test plans, develop RTL behavioral code and debug, logic synthesis and timing, assist with floor planning, place & route, back-end IC checks, production engineering, post-silicon debug
- Work with CAD/CAE/DV teams to develop design tools and automation infrastructure

REQUIRED QUALIFICATIONS:

- BSEE/CS or higher and 5+ years of hands-on digital CMOS IC/SoC Design experience
- Demonstrated ability to develop digital ICs to tape out
- Deep familiarity with either Verilog and/or System Verilog RTL development including logic synthesis and static timing analysis
- Good organization; written and verbal communication skills

DESIRED QUALIFICATIONS:

- Top-level digital architecture capability including contributions to design specification, process/IP selection, and design partitioning
- Knowledge of digital designer verification, both UVM and/or formal (e.g., Jasper)
- Knowledge of floor planning, automated place & route, CTS, LVS, DRC
- Knowledge of IC product testing (ATPG, JTAG, MBIST, LBIST)
- Knowledge of both Bulk and FinFet CMOS processes, Spice analysis thereof
- Ultra-low power digital design techniques, including clock and power gating